REMARKS

This is a complete and timely response to the non-final Office Action mailed June 4, 2007. Claims 1 and 3-13 are pending in the application. Claim 2 is canceled. Claims 1, 3, 5-7 and 9-13 are amended. The subject matter of amended claim 1 is supported in at least original claim 2 (canceled), FIG. 3, and the related detailed description. Claims 3, 5-7 and 9-13 are amended to provide proper antecedent basis for all elements in the claims. Accordingly, no new matter is added.

In view of the foregoing amendment and following remarks, reconsideration and allowance of the present application and claims are respectfully requested.

Allowable Subject Matter

Applicant gratefully acknowledges the indication in the Office Action that claims 4-13 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. However, Applicant believes that claim 1, as amended, is patentable over the cited reference.

Rejections Under 35 U.S.C. § 102

Claims 1-3 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent Application Publication No. 2003/0233523 to Jamil *et al.* (hereafter *Jamil*).

Claim 2 is canceled. Accordingly, the rejection of claim 2 is rendered moot.

A proper rejection of a claim under 35 U.S.C. § 102 requires that a single prior art reference disclose each element of the claim. *See, e.g., W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983). Anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *See, e.g., In re Paulsen,* 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Alternatively, anticipation requires that each and every element of the claimed invention be embodied in a single prior art device or practice. *See, e.g., Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992). The test is the same for a process. Anticipation requires identity of the claimed process and a process of the prior art. The claimed

process, including each step thereof, must have been described or embodied, either expressly or inherently, in a single reference. *See, e.g., Glaverbel S.A. v. Northlake Mkt'g & Supp., Inc.,* 45 F.3d 1550, 33 USPQ2d 1496 (Fed. Cir. 1995). Those elements must either be inherent or disclosed expressly. *See, e.g., Constant v. Advanced Micro-Devices, Inc.,* 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988); *Verdegaal Bros., Inc. v. Union Oil Co.,* 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987). Those elements must also be arranged as in the claim. *See, e.g., Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989); *Carella v. Starlight Archery & Pro Line Co.*, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986). For anticipation, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. *See, e.g., Scripps Clinic & Res. Found. v. Genentech, Inc.,* 927 F.2d 1565, 18 USPQ2d 1001 (Fed. Cir. 1991).

Accordingly, the single prior art reference must properly disclose, teach or suggest each element of the claimed invention. Applicant's claim 1, as amended, includes at least one feature that is not disclosed, taught or suggested by *Jamil*.

The Office Action states that:

> As per claim 1, Jamil teaches a system comprising
> - shared system registers (i.e. the part of the shared storage, 190, 290 and 490 in Figs. 1, 2 and 4, respectively), each register including one or more bits defining an access protocol (i.e. the Status shown in Fig. 4), and one or more bits representing data (i.e. 411-430 in Fig. 4); and
> - N processors (i.e. processors 101 and 102 in Fig. 1), N≥2, where n is an integer (i.e. n is 2 in Fig. 1), each accessing the registers (i.e. as shown in Fig. 4) (e.g. see the abstract and Figs. 1-2 and 4).
>
> As per claim 2, Jamil teaches the claimed invention as described above and furthermore, Jamil teaches that the access protocol including a configurable access type for each N processors (i.e. status listed for each shared register as shown in Fig. 4).
>
> As per claim 3, Jamil teaches the claimed invention as described above and furthermore, Jamil teaches that the access type being selected from a group that includes READ, READ/CLEAR, READ/SET, and READ/WRITE, is inherently embedded in the system taught by Jamil prior art because based on the status listed in Fig. 4 appropriate access type can be derived.

See Office Action pp. 2-3.

Applicant's independent claim 1, as amended, includes "shared system registers, each register including one or more bits defining an access protocol," and "said one or more bits defining the access protocol include one or more bits that define a register access type for each N processors."

Applicant respectfully submits that at least these features are not disclosed by *Jamil*. *Jamil* discloses, in one embodiment of a coherent storage hierarchy, illustrated in FIG. 4,

> a scalable presence encoding to be held in a presence portion of storage for a corresponding data portion that further reduces backward inquiries and potentially avoids unnecessary invalidation requests.

See *Jamil*, paragraph 0042.

Applicant respectfully submits that *Jamil* shows data portions (411 through 430) and storage control 491 in a shared storage 490. Storage control 491 includes status and presence information that corresponds to each respective data portion. A data portion, which is separate from storage control 491, does not disclose, teach or suggest shared system registers that define an access protocol including one or more bits that define a register access type for *each* N processors, as claimed in claim 1.

Applicant's system is structurally different from the coherent storage hierarchy of *Jamil*. Applicant's system includes shared system registers that include one or more bits defining an access protocol and one or more bits representing data. The one or more bits defining the access protocol include one or more bits that define a register access type for each N processors.

In marked contrast with Applicant's shared system registers, which include one or more bits that define a register access type for each N processors, *Jamil* discloses a storage control that includes status identifiers and a presence encoding corresponding to a data portion.

First, *Jamil* shows separate data portions (411-430) and corresponding status and presence information in storage control 491. Separate data portions and corresponding status and presence information in a storage control cannot anticipate a shared system register.

Second, *Jamil* shows status identifiers (exclusive-dirty (ED), shared (S), modified (M), invalid (I), and exclusive-clean (EC)) suited for resolving sharing ambiguities in a coherent storage hierarchy. *Jamil* does not disclose, teach or suggest a shared system register that includes one or more bits that define a register access type. The ED, S, M, I and EC status identifiers, disclosed by *Jamil*, which can be used to resolve data ambiguity in a coherent storage hierarchy, do not correspond or map to Applicant's register access type(s).

Third, *Jamil* shows presence encoding in a portion of storage control 491 that corresponds to the status identifier and a separately located data portion. In accordance with paragraph [0044] a presence portion holds a presence encoding of (0001, 0100, 1000, 0010) indicating that a corresponding respective data portion (411, 413, 415, 418) has been provided to a respective private storage (410, 440, 480, 420). Thus, *Jamil* shows presence encoding that defines a corresponding private storage. A private storage is not a processor.

Accordingly, for at least these reasons, *Jamil* does not disclose, teach or suggest a shared system register that includes one or more bits that define a register access type for *each* N processors, as recited in Applicant's independent claim 1. Consequently, *Jamil* does not anticipate the system of amended claim 1. Accordingly, Applicant respectfully submits that claim 1 is allowable and the rejection under 35 U.S.C. § 102(e) should be withdrawn.

Further, Applicant respectfully submits that dependent claim 3 is allowable for at least the reason claim 3 depends directly from allowable independent claim 1. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988) (Citations omitted).

CONCLUSION

For at least the reasons set forth above, Applicant respectfully submits that pending claims 1 and 3-13 are allowable over the cited art of record and the present application is in condition for allowance. Accordingly, a Notice of Allowance is respectfully solicited. Should the Examiner have any comments regarding the Applicant's response, Applicant requests that the Examiner telephone Applicant's undersigned attorney.

Respectfully submitted,

SMITH FROHWEIN TEMPEL GREENLEE BLAHA LLC

By: /Robert A. Blaha/
Robert A. Blaha
Registration No. 43,502
(770) 709-0069